Low Power VLSI Design for Power and Area Effective Utilisation of Carry Select Adder

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ABSTRACT

Design of power-efficient and high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position.

The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input , then the final sum and carry are selected by the multiplexers (mux). The existing modified SQRT CSLA is to use Binary to Excess-I Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption with slightly increase in the delay. The basic idea of this work is to use Common Boolean logic(CBL) instead of BEC in the regular CSLA to achieve high speed and low power consumption ane even the area consumed by the each system.

Key words :Power, cbl, Bec, csla.

I INTRODUCTION

The major speed limitation in any adder is in the production of carries and many authors have considered the addition problem. The basic idea of the proposed work is using n-bit Binary to Excess-1 Converters (BEC) to improve the speed of addition. This logic can be implemented With Carry Select Adder to Achieve Low Power and Area Efficiency. The proposed 32-bit Carry Select Adder compared with the Carry Skip Adder (CSKA) and Regular 32-bit Carry Select Adder.

The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin = 0 and Cin = 1, then the final sum and carry are selected by the multiplexers (mux). The entire work performed by usage of Binary to Excess-1 Converter (BEC) instead of RCA with Cin = 1 in the regular CSLA to achieve lower power consumption The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Ripple Carry Adder (RCA). A structure of 4-bit BEC and the truth table is shown in Fig.1.1 and Table 1 respectively.

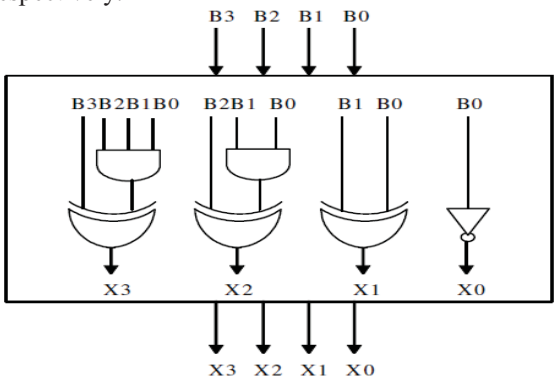

Fig. 1.1:4-bit

Binary to Excess-1 Converter (BEC)

B[3:0]	X[3:0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

Table.1 : Functional Table of 4-Bit BEC

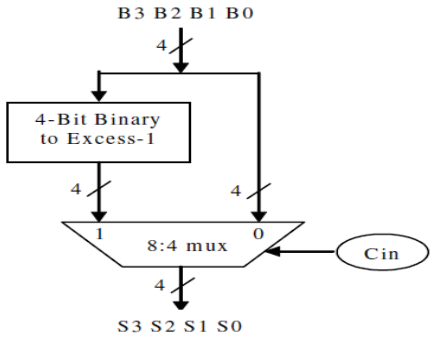

Fig.1.2. 4-b BEC with 8:4 mux

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How the goal of fast addition is achieved using BEC together with a multiplexer (mux) is described in Fig.1.2, one input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the Mux is the BEC output. This produces the two possible partial product results in parallel and the Muxes are used to select either BEC output or the direct inputs according to the control signal Cin.

The Boolean expressions of 4-bit BEC are listed below, (Note: functional symbols, ~ NOT, & AND, ^ XOR).

X0 = ~ B0
X1 = B0 ^ B1
X2 = B2 ^ (B0 & B1)
X3 = B3 ^ (B0 & B1 & B2)

The AND, OR, and Inverter (AOI) implementation of an XOR, 2:1 MUX, FA are shown in below. The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block.

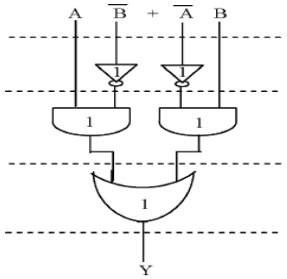


Fig.1.3:Delay and Area evaluation of an XOR gate.

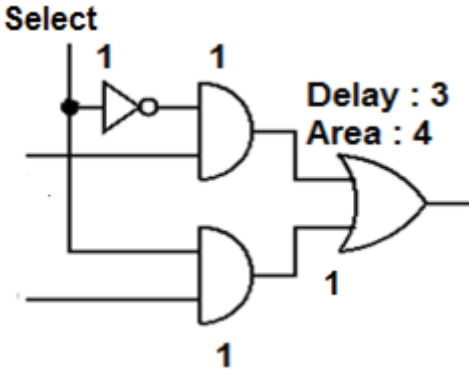


Fig.1.4:Delay and Area evaluation of an 2:1 Mux gate.

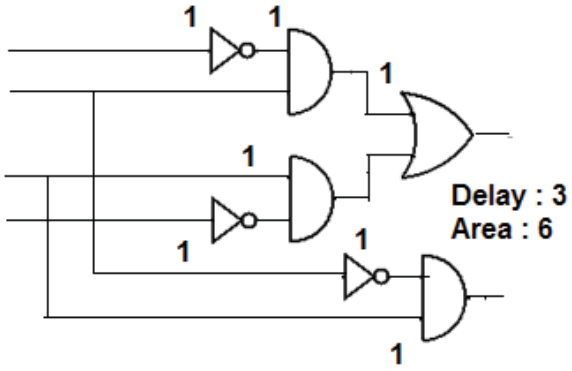


Fig.1.5:Delay and Area evaluation of an Full Adder.

A. Ripple carry adder(RCA)

Ripple carry adder is an n-bit adder built from full adders. Fig 2.1 shows a 4-bit ripple carry adder. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. Even though this is a simple adder and can be used to add unrestricted bit length numbers, it is however not very efficient when large bit numbers are used.

One of the most serious drawbacks of this adder is that the delay increases linearly with the bit length. The worst-case delay of the RCA is when a carry signal transition ripples through all stages of adder chain from the least significant bit to the most significant bit, which is approximated by:

T = (n-1) tc + ts

Delay :

The latency of a 4-bit ripple carry adder can be derived by considering the worst-case signal propagation path. We can thus write the following expressions:

TRCA-4bit = TFA(A0,B0→Co)+T FA (C in→C1)+TFA (Cin→C2)+ TFA (Cin→S3)

And, it is easy to extend to k-bit RCA:

TRCA-4bit = TFA(A0,B0→Co)+(K-2)* TFA (Cin→Ci)+ TFA (Cin→Sk-1).

Drawbacks :

Delay increases linearly with the bit length and Not very efficient when large bit numbers are used.

B: Carry Select Adder(CSLA)

A carry-select adder is divided into sectors, each of which – except for the least-significant –performs two additions in parallel, one assuming a carry-in of zero, the other a carry-in of one. A four bit carry select adder

generally consists of two ripple carry adders and a multiplexer. The carry-select adder is simple but rather fast, having a gate level depth of O(√n) . Adding two n-bit numbers with a carry select adder is done with two adders (two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one.

In the N-bit carry ripple adder, the delay time can be expressed as:

TCRA = (N-1) Tcarry + Tsum

In the N-bit carry select adder, the delay time is:

TCSA = Tsetup + (N/M) Tcarry + MTmux + Tsum

In our proposed N-bit area-efficient carry select adder, the delay time is:

Tnew = Tsetup + (N-1) Tmux + Tsum

The carry select adder comes in the category of conditional sum adder. Conditional sum adder works on some condition. Sum and carry are calculated by assuming input carry as 1 and 0 prior the input carry comes. When actual carry input arrives, the actual calculated values of sum and carry are selected using a multiplexer.

II Basic Structure Of Regular SQRT CSLA (DUAL RCA)

The basic square root Carry select adder has a dual ripple carry adder with 2: 1 multiplexer the main disadvantage of regular CSLA is the large area due to the multiple pairs of ripple carry adder. The regular 16-bit Carry select adder is shown in Fig. 1. It is divided into five groups with different bit size RCA. From the structure of Regular CSLA, there is scope for reducing area and power consumption. The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of the output carry and sum. The selection is done by using a multiplexer . Internal structure of the group 3 of regular 16- bit CSLA is shown Fig.2.By manually counting the number of gates used for group 3 is 87 (full adder, half adder, and multiplexer) and 13ns delay. One input to the mux goes from the RCA with Cin=O and other input from the RCA with Cin=1.

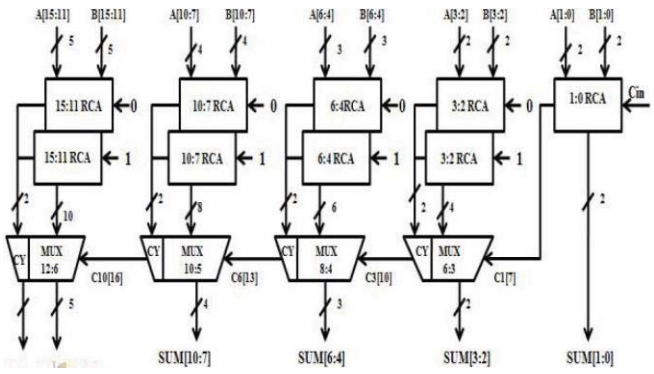


Figure 1: Regular 16-bit SQRT CSLA

A. Drawback :

The problem in CSLA design is the number of full adders are increased then the circuit complexity also increases. The number of full adder cells are more thereby power consumption of the design also increases.
Number of full adder cells doubles the area of the design.

B. MODIFIED SQRT CSLA USING BEC

The modified Carry select adder has a single ripple carry adder with Binary to Excess-I converter, which replace the ripple carry adder with Cin=l, in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+ I -bit BEC is required .A structure and the function table of a 4-b BEC is shown in Table I, respectively. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols (NOT, & AND, I\XOR).

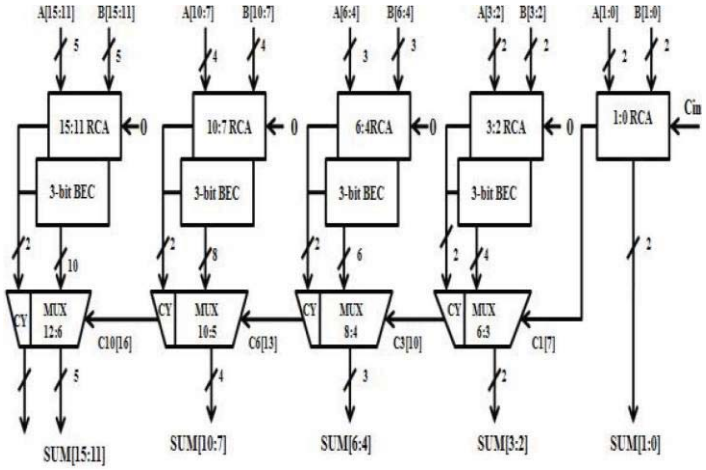


Figure 2: Modified 16-bit SQRT CSLA

III: Drawbacks Of CSLA Using BEC:

A Advantages:

To evaluate the performance, The Regular SQRT CSLA has the disadvantage of more power consumptions and occupying more chip area. So, to improve the power consumption and chip area the Modified 16-b SQRT CSLA has been proposed here.

IV Common Boolean Logic (CBL)

Here, an area-efficient carry select adder by sharing the common Boolean logic term to remove the duplicated adder cells in the conventional carry select adder. In this way, it save many transistor counts and achieve a low Power. Through analyzing the truth table of a single-bit full adder, To find out that the output of summation signal as carry-in signal is logic "0" is the inverse signal of itself as carry-in signal is logic "I ". As illustrated as two dotted circles in the truth table of Fig. 3, By sharing the common Boolean logic term in summation generation, a proposed carry select adder design is illustrated in Fig. 6. To share the common Boolean logic term, it only needs to implement one OR gate with one INV gate to generate the Carry signal and summation signal pair. Once the carry-in

signal is ready, then select the correct carry-out output according to the logic state of carry-in signal.

C_{in}	A	B	S0	C0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 4.1: The truth table of single-bit full-adder and single bit FA with common Boolean logic

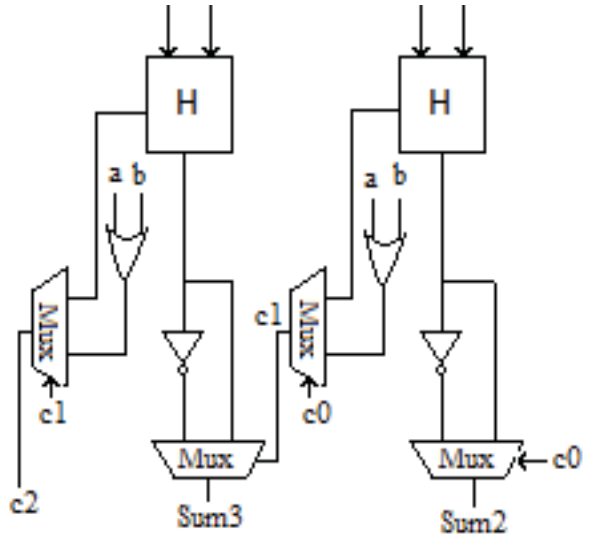


Figure 4.1: internal diagram of 2 bit csla using Common Boolean Logic

As compared with the Modified Carry Select adder, the proposed CSLA is little bit faster, but the speed is nearly equal to the Regular CSLA. The delay time in our proposed adder design is also proportional to the bit number N; however, the delay time of multiplexer is shorter than that of full adder. The Proposed CSLA is Area efficient & low power, but the speed equal to the Regular CSLA.

A. Proposed CSLA Architecture

This method replaces the BEC add one circuit by Common Boolean Logic. The output waveform of full adder for carry in signal is 'I ' is generate summation and carry signal by just using an TNV and OR gate. It is shown in fig.5.

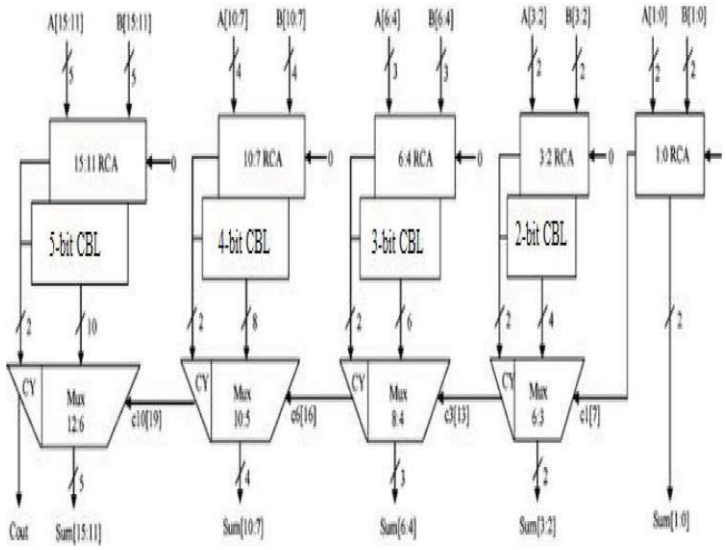


Figure 4.2: The Proposed 16-bit SQRT CSLA using CBL The Summation and carry signal for FA which has Cin=l, Generate by INV and OR gate. Through the multiplexer, we can select the correct output result according to the logic state of carry-in signal.

Internal structure of the of Proposed CSLA is shown Fig. 6. One input to the mux goes from the RCA block with Cin=O and other input from the CBL

V . RESULTS

COMPARISION OF ADDERS

A: CSLA USING DUAL RCA

NO. Of Bits ADDER	4	8	16
AREA (GATE COUNT)	91	108	269
POWER(mW)	4	6	7
DELAY(ns)	13.97	18.42	24.93
Memory USED	163540	164244	164372

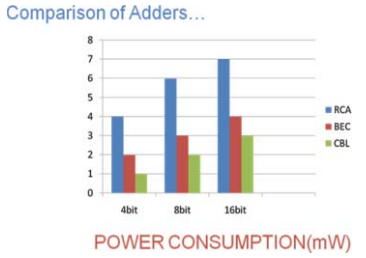
B: CSLA USING BEC

NO. Of Bits ADDER	4	8	16
AREA (GATE COUNT)	48	138	297
POWER(mW)	2	3	4
DELAY(ns)	13.648	16.436	22.11
Memory USED(Kb)	163860	164308	165204

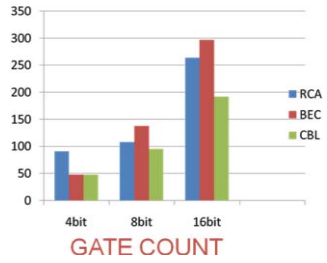
C: CSLA USING CBL

NO. Of Bits ADDER	4	8	16
AREA (GATE COUNT)	48	96	192
POWER(mW)	1	2	3
DELAY(ns)	13.90	20.394	33.738
Memory USED	164052	164628	164316

V. POWER



A. GATE COUNT



B. DELAY

VI Conclusion:

In this project a modified approach is introduced to reduce the area, power and delay of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area, total power and also reduces the delay. A regular CSLA uses two copies of the carry evaluation blocks, one with block carry input is zero and other one with block carry input is one. The Regular SQRT CSLA has the disadvantage of power consumption, chip area. The modified SQRT CSLA reduces the area and power when compared to regular CSLA with increase in delay by the use of Binary to Excess-I converter. The proposed method, which reduces the delay, area and power than regular and modified CSLA by the use of Common Boolean Logic.

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